Frank Qiu

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Objective

Seeking an internship where I can leverage my expertise in systems, networking, and machine learning.
I enjoy taking a bottom-up approach, from low level architecture and operating system all the way to the upper layer applications linke machine learning. Currently, I'm working on a networking system that enhances ML training through just-in-time gradient compression via packet trimming.

Education

Purdue University **September 2024 –**
Ph.D. in Electrical and Computer Engineering, advised by Prof. Xiaoqi Chen *West Lafayette, Indiana, US*

Shanghai Jiao Tong University **September 2020 – June 2024**
B.E. in Computer Science and Technology (Zhiyuan Honors Program), ACM Class *Shanghai, China*

Skills

Engineering: Exceptional code style, document writing, and version control. Proficient in both Windows and Linux environments. Experienced with industry toolchains and documentation (*Vivado*).

Programming: Proficient in algorithm, data structure, modern programming language features (*e.g. C/C++, Rust, Python, Java*), HDL (*Verilog*), database (*MongoDB*), utility programs (*e.g. MATLAB, Visual Basic, Unity, Processing*).

Administration: Served as the class representative and public relation officer of Zhiyuan honors college student union.

Experience

Distributed Systems Laboratory, University of Pennsylvania **August 2023 – December 2023**
Research Assistant, advised by Prof. Vincent Liu *Philadelphia, Pennsylvania, US*

- Investigated co-design of the FPGA-based SmartNIC and the host networking stack.
- Leverage idle PCIe transactional bandwidth to mitigate host congestion.
- Optimize tail latencies for high-level applications.

BCMI Laboratory, Shanghai Jiao Tong University **July 2022 – July 2023**
Research Assistant, advised by Prof. Li Niu *Shanghai, China*

- Proposed a deep learning network of image harmonization guided by reflectance.
- Designed a diverse reflectance generation network to predict a variety of plausible foreground reflectances.
- Enabled multiple plausible image harmonization results using the outputs from the generation network.

Zhiyuan College, Shanghai Jiao Tong University **September 2021 – June 2023**
Teaching Assistant for lectures, design & grading of homeworks, projects, exams *Shanghai, China*

- CS1953 Programming, Fall 2021
- CS1952 Programming Practice, Summer 2022
- CS2951 Computer Architecture, Fall 2022
- CS2952 Operating System, Spring 2023

Selected Course Projects

RISC-V Out-of-Order Execution CPU | *CPU, FPGA, Verilog, RISC-V*

- Designed an FPGA circuit of a RISC-V (RV32I instruction set) out-of-order execution CPU of Tomasulo algorithm, written in Verilog, tested on AX7035 board.

CJ Compiler | *Compiler, LLVM IR, RISC-V, Java*

- Engineered a compiler that compiles a C-and-Java-like language Mx* to LLVM Intermediate Representation and RISC-V assembly (RV32M instruction set), written in Java.

Awards

SJTU Merit Scholarship; Zhiyuan Honors Scholarship **2020, 2021, 2022, 2023**
National Olympiad in Informatics in Provinces, Senior Group, Shanghai Area, First Prize **2017, 2018**